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MAHLTIG MANAGEMENT- UND
BETEILIGUNGSGESELLSCHAFT MBH

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

In re APPLICATION OF MAHLTIG MANAGEMENT- UND BETEILIGUNGSGESELLSCHAFT MBH FOR AN ORDER PURSUANT TO 28 U.S.C. § 1782 GRANTING IT LEAVE TO OBTAIN DISCOVERY FROM INTEL CORP. FOR USE IN FOREIGN PROCEEDINGS	Case No. 3:18-mc-80037-WHO **MAHLTIG MANAGEMENT'S AND INTEL'S JOINT STATEMENT REGARDING DISCOVERY DISPUTE**

Mahltig Management- und Beteiligungsgesellschaft mbH ("Mahltig Management") asks the Court for an expedited telephonic hearing to resolve disputes that have arisen since the Magistrate Judge ruled on the application of Mahltig Management for leave to serve subpoenas on Intel Corp. ("Intel"). Pursuant to the Court's standing order on discovery disputes, the parties met and conferred via multiple email exchanges, and over the telephone on June 5, 2018.

I. Mahltig Management's Position

With regard to Request 1 in the subpoena as modified by the Court, Intel has failed to disclose registers or other memory to which the ME Processor has indirect access, for example and without limitation, devices (e.g. USBs and SSDs) connected via the PCIe bus or via the SMbus. Intel confirmed during the June 5, 2018 call that it had not yet produced such information. Mahltig Management has strong reasons to believe that such documents exist, and in an email dated May 24, 2018, it provided Intel with the example of the NVMe specification, which shows that SSDs can be accessed via the SMBus, to which the ME is connected. Further, in a figure printed in *Intel Technology Journal* (Vol. 12, No. 4, at p. 20) a connection is shown between the Intel ME and two components called "VE" and CSB." Intel has not, as far as Mahltig Management can determine, [1] produced information regarding registers in these components.

Request 2 specifically calls for documents sufficient to show whether the PC processor and/or the ME Processor can be programmed to read or write certain registers, including, e.g., registers in hard disk controllers, regardless "whether or not such programming would usually be authorized by Intel," i.e., whether or not they actually are programmed in that way. In the June 5 telephone call, Intel revealed that it had construed Request 2 to apply to registers that the ME can be ***and is*** programmed to access rather than to registers that it *can* be programmed to access.

[1] Part of the difficulty is that Intel produced what appear to be summary tables, perhaps created for the purpose of the production, rather than the underlying documents. The summary tables lack context that would assist Mahltig Management's lawyers in understanding what Intel has produced. In light of the Court's decision overruling Mahltig Management's objection to the Magistrate Judge's decision on the protective order, Mahltig Management is in a difficult position: the technical experts who have knowledge of the context that would allow them to understand Intel's production cannot see it. Mahltig Management therefore requests that the Court order Intel to produce the *underlying documents* (data sheets, technical documentation, and the like) that identify the registers responsive to Request 1. This will maximize the likelihood that Mahltig Management's counsel will be able to understand the production properly.

Construing the request as Intel does is contrary to its plain meaning and deprives Mahltig Management of important discovery. In any case, the figure referenced above shows there is a connection—whether direct or indirect is immaterial—between the ME and the SATA controller, which is expressly within the definition of "hard disk controller" in the subpoena. Yet Intel has produced no documents regarding this connection, which appears in Intel's own literature.

Mahltig Management claims that PCs that incorporate Intel's ME technology infringe its patent if they can be programmed to access these registers, whether or not they are thus programmed. Request 2 also calls specifically for analyses carried out by third parties including but not limited to Positive Technologies. There is no dispute that the Positive Technologies analysis exists, and we understand that the analysis analyzed a chipset (PCH) that Intel made available commercially rather than, for example, a prototype. But Intel says it need not produce the analysis, because the request does not call for the production of "all documents" but only "documents sufficient to show" the requested information. Mahltig Management believes, based on publicly-available information, that the Positive Technologies analysis shows that the ME can manage all devices inside the PCH (Chipset), which would include SSDs and USBs. So the issue is not Intel's choice to produce one document rather than another, but rather its failure so far to produce any document with the required information. The Positive Technologies analysis should be produced. The same analysis applies to a presentation by Bulyigin, an Intel employee, which shows a connection between the ME and an SSD.

Intel proposes to complete its search for documents responsive to Request 1 by the end of June, that is, after an upcoming substantive hearing in the *Lenovo* case scheduled for June 28. The Court's prior order required production of responsive documents by May 8, 2018, more than a month ago. It is important that Intel not be allowed to run out the clock. This is particularly important because Mahltig Management intends to argue in the *Lenovo* case that in the other German proceeding ("the *Acer case*"), Intel's misstatement of the facts contributed to the *Acer* court's erroneous decision on infringement, and that the *Lenovo* court should not follow the *Acer* decision. In particular, in the *Acer* case, Mr. Haft, Intel's European counsel, stated: "… [T]he ME cannot access the hard disk - also not via the SATA controller. There is neither a corresponding

hardware connection, nor a corresponding programming. The plaintiff's speculation to the contrary … is absurd." Yet in the *Lenovo* case, Mr. Haft, perhaps in light of this pending discovery proceeding, made no similar statement. It is essential that Mahltig Management be able to rebut the statements Intel made to the *Acer* court in connection with the *Lenovo* case.

II. Intel's Position

There is no reason for Mahltig to burden the Court or Intel with this expedited but strawman filing. The problem is not the adequacy of Intel's production. Intel has produced tables showing the information sought in Requests 1 & 2, and it did so by the May 8 deadline. Rather, the problem is that Mahltig is unhappy with what those tables show. But facts are facts, and no amount of complaining and conjecture by Mahltig can change them.

Request 1 seeks documents "sufficient to identify the registers and other memory to which the ME Processor has direct or indirect access"; Request 2 seeks documents "sufficient to show" whether an ME processor can be programmed to read or write to registers on a hard disk, SSD, or USB mass storage device. Intel produced tables identifying the registers that are accessible by its ME processors. That information responds not only to Request 1, but also to Request 2: The ME processor cannot access registers on any of the listed storage devices, which necessarily means that it cannot be programmed to read or write to them.

Mahltig is unhappy with those facts and contends that the tables must be incomplete. Since Intel produced those tables on May 8, Mahltig has pointed to publicly available documents that it thinks shows that the ME processor can access additional registers. Each time Intel has gone back to confirm that the ME processor cannot access those registers. Those efforts have involved engineers around the world and required Intel to confirm negatives, which takes time. And each time Intel has shown that a Mahltig hypothesis is wrong, Mahltig comes up with a new one. The latest example is Mahltig's reference above to a 2008 article mentioning registers on a "CSB" (Crypto Security Block) and a "VE" (Virtualization Engine). Mahltig first raised this issue only last week when it knew Intel's counsel was on vacation overseas. Nevertheless, Intel has already confirmed that it did not in fact implement the CSB functionality and thus that there are no additional registers to identify for that functionality. Although not required to do so, Intel is

searching for contemporaneous documentation of that fact (which is taking time given how old it is). Likewise, Intel's initial investigation indicates that the VE functionality was never implemented either, but Intel is still confirming that fact. Intel will inform Mahltig as soon as it does so. Intel is hardly trying to "run out the clock." [2]

Mahltig's incorrectly asserts that Intel has proposed completing its production by the end of June. Intel made its production on May 8, as ordered. That production identified the registers accessible by the earliest version of the ME at issue and by the current version. As Intel has told Mahltig, the registers accessible by the intervening versions are a subset of the registers accessible by the current version and do not include registers that are on the hard disk, SSD, or USB storage device. Nevertheless, in the interests of completeness, Intel offered to produce tables for the intervening versions. Intel anticipates doing so by June 30. (The process has been slowed because Intel has had to divert its efforts to respond to Mahltig's *seriatim* assertions that various registers are missing from the tables.)

Mahltig complains that Intel has not yet produced information about registers to which the ME processor has indirect access. Not true. Intel has confirmed to Mahltig that the tables produced on May 8 include all such registers.

Mahltig also seeks (*supra*, note 1) to expand the scope of the first request by demanding the "underlying documents" so that it can understand the "context" of the tables that Intel produced. That new request should be rejected. First, on its face, Request No. 1 is limited to documents "sufficient to identify" the registers. Intel's production does precisely that. In ordering a "sharp curtailment" of Mahltig's "unduly intrusive and burdensome" subpoena, Judge Cousins quashed requests that were not limited to documents "sufficient to show." [Dkt. No. 32 at 8-9; Dkt. No.1 at 14-15 (Request Nos. 10-12)] Second, this is another attempt by Mahltig to go on a fishing expedition. Mahltig does not specify any information it needs for "context." In fact, Intel already put the tables in "context" by identifying the functionalities to which the registers relate. Intel further told Mahltig that none of the registers is on the relevant storage devices. In other

[2] Moreover, any time pressure is entirely of Mahltig's own making. As Magistrate Judge Cousins found, Mahltig showed a "particularly disturbing" "lack of diligence" in failing to seek the requested discovery earlier. [Dkt. No. 32 at 6]

words, because the registers do not relate to Mahltig's patent claims, Mahltig has no need for further information about them. Third, Mahltig's new request would impose an undue burden by requiring Intel to redact thousands of pages of confidential information. The information in the tables was gathered from numerous documents that collectively contain thousands of pages of Intel trade secrets irrelevant to Mahltig's subpoena. As Intel has consistently explained, it is concerned that Mahltig will misuse its confidential information, and it is unwilling to disclose trade secrets not called for by the subpoena.

Mahltig erroneously complains that Intel has read Request 2 as limited to "registers that the ME can be ***and is*** programmed to access rather than to registers that it *can* be programmed to access." Intel has no idea why Mahltig thinks that, but it is incorrect. Intel has always read that request as applying to registers that the ME can be programmed to access, regardless of whether it has been programmed to do so. The parties are not in disagreement.

Mahltig next asks that Intel be ordered to produce an analysis prepared by Positive Technologies. But Judge Cousins quashed Mahltig's document request that called for Intel to produce that analysis. [Dkt. No. 32 at 8-9; Dkt. No.1 at 14 (Request 9)][3] Mahltig did not object to Judge Cousins' order quashing that request, and it is improper for Mahltig to seek it through the back door. And, as already discussed, Intel has produced all of the register information called for by Requests 1 and 2. Finally, Mahltig wrongly asserts that European counsel has dropped the argument that the ME cannot access the hard disk. To the contrary, Lenovo's most recent submission from May 22 states: "[T]he ME processor is particularly unable to access the hard disk or the SSD (solid state drive), not even via the SATA interface." [4] The Court should reject Mahltig's request for additional discovery.

Dated: June 20, 2018 /s/ Germain D. Labat /s/Timothy J. Franks

[3] Mahltig told the Court that Request 9 ("The documents provided to Intel on June 7 and July 6, 2017 that led to the publication of security advisory SA-00086") sought the Positive Technologies analysis. [Dkt. No. 1 at 14; Dkt. No. 2 at 16; Dkt. No. 5 at 30-36]

[4] Mahltig also makes a puzzling request that Intel produce a presentation by Intel employee Bulygin. In fact, Mahltig already has that document and submitted it in the European actions. [Dkt. No. 25-2 at ¶ 11 and Ex. 2] In any event, no responsive information from the presentation was left out of Intel's production.